REMARKS

Reconsideration of this application is respectfully requested in view of the foregoing amendment and the following remarks.

By the foregoing amendment, applicant has amended claims 1 and 8-10, and added new claims 17-19. Claims 1-11 and 17-19 are currently pending, claims 12-16 having been withdrawn from consideration.

Claim 8 has been amended to overcome the rejection under 35 U.S.C. 112, second paragraph. Accordingly, reconsideration and withdraw of that rejection is respectfully requested.

In the Office Action mailed August 29, 2002, the Examiner rejected the pending claims as unpatentable over the prior art. To the extent that these rejections might still be applied to the claims as amended, they are respectfully traversed as follows.

According to amended claim 1, a method of making a semiconductor device comprises the steps of: mounting a semiconductor chip on a lower conductor, with first solder material applied between the chip and the lower conductor; positioning an upper conductor on the chip, with second solder material applied between the chip and the upper conductor; heating up the first and the second solder materials beyond melting points of the respective materials; and solidifying the first and the second solder materials; wherein the first solder material is caused to solidify earlier than the second solder material in the solidifying step.

The claimed method is advantageous for appropriately securing the semiconductor chip to the lower conductor since the solidification of the first solder material occurs earlier than that of the second solder material. In the solidifying step, the first solder material between the lower

conductor and the chip solidifies while the second solder material between the chip and the upper conductor is still in a molten state. Thereafter, the second solder material solidifies. In this manner, the chip is secured to the lower conductor before it is secured to the upper conductor. Accordingly, it is possible to prevent the chip from being unduly raised toward the upper conductor, even in the case where the chip has a protruding upper electrode on its upper surface.

As noted in the Office Action, Froloff et al. teaches solder materials each having a different melting point. However, Froloff et al. does not teach or remotely suggest using one of the materials for the first solder and another having a different melting point for the second solder. Moreover, Froloff et al. does not teach or remotely suggest using a lower melting point solder material for the first solder and a higher melting point solder material for the second solder. Furthermore, Froloff et al. does not teach anything about the order of solidification. Specifically, Froloff et al. does not teach that the first solder material is caused to solidify earlier than the second solder material in the solidifying step. According to Froloff et al., soldering is performed in a simple process, which per se is known for the use of soft solder (column 4, line 24-27).

Yamamoto et al. and Williams et al. also do not teach anything about the order of solidification.

During the examination process, the PTO has the burden under § 103 to establish a prima facie case of obviousness. In re Fine, 5 USPQ2nd 1596, 1598 (Fed. Cir. 1988). The PTO "can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the

relevant teachings of the references." Id. It is not sufficient to find a prima facie case of obviousness on the basis that the prior art reference could be modified or may be capable of being modified to operate in the manner claimed. In re Mills, 16 USPQ2nd 1430, 1432 (Fed. Cir. 1990). In order to establish obviousness, there must be a suggestion or motivation in the reference to do so. Id. See also In re Gordon, 221 USPQ 1125, 1127 (Fed. Cir. 1984) (prior art could both be turned upside down without motivation to do so). It is evident form Federal Circuit case law that the preferred method of establishing motivation or suggestion for modification is to rely on a suggestion within the primary reference or to find such a suggestion in a teaching reference. As stated in Fine, "'To imbue one of ordinary skill in the art with knowledge of the invention in suit, when no prior art reference or references of record convey or suggest that knowledge, is to fall notion to the invidious effect of a hindsight syndrome.'" 5 USPQ2nd at 1600 (quoting W.L. Gore & Assoc. v. Garlock, Inc., 220 USPQ 303, 312-13). Accord Mills, 16 USPQ2nd at 1432: In re Demenski; 230 USPQ 313, 315 (Fed. Cir. 1986) (reversing rejection of claims where no suggestion existed in the prior art references to make proposed design modification and rejecting Board's argument as hindsight that the proposed modification was "common practice"). See also Northern Telecom, Inc. v. Data Point Corp., 15 USPQ2nd 1321, 1323 (Fed. Cir. 1990), (rejecting "routine design choice" absent any suggestion in the prior art to make proposed modification).

For the reasons discussed herein, applicant submits that the Examiner has not made the requisite showing of proper motivation to combine the references. The mere fact that a prior art reference could be modified to meet the claim is insufficient to establish obviousness. Here the

objective evidence presented above teaches away from any motivation or suggestion to make modifications required.

In view of the foregoing all of the claims in this case are believed to be in condition for allowance. Should the Examiner have any questions or determine that any further action is desirable to place this application in even better condition for issue, the Examiner is encouraged to telephone applicants' undersigned representative at the number listed below.

Respectfully submitted,

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Date: November 27, 2002

Attachments: Amended Claims w/ Markings

MDB/lrhj

VERSION WITH MARKINGS TO SHOW CHANGES MADE TO CLAIMS

1. (Amended) A method of making a semiconductor device, the method comprising the steps of:

mounting a semiconductor chip on a lower conductor, with first solder material applied between the chip and the lower conductor;

positioning an upper conductor on the chip, with second solder material applied between the chip and the upper conductor;

heating up the first and the second solder materials beyond melting points of the respective materials; and

solidifying the first and the second solder materials; wherein the first solder material is caused to solidify earlier than the second solder material[.] in the solidifying step.

8. (Amended) The method according to claim [7] 6, wherein the upper conductor comprises upper lead portions [divided into first and second groups].

9. (Amended) The method according to claim [8] 14, further comprising the step of removing at least one of the lower and the upper lead portions from the frame.

10. (Amended) The method according to clam [8] 14, wherein the frame comprises first and second common bars parallel to each other, the upper lead portions being divided into first and second groups, the upper lead portions in the first group extending from the first

common bar toward the second common bar, the upper lead portions in the second group extending from the second common bar toward the first common bar.

17. (New) The method according to claim 1, further comprising the step of preparing a conductive frame which includes a first conductive pattern and a second conductive pattern, the first conductive pattern including the lower conductor, the second conductive pattern including the upper conductor.

18. (New) The method according to claim 12, wherein the lower conductor comprises a die pad portion and lower lead portions extending from the die pad portion on which the semiconductor chip is to be mounted.

19. (New) The method according to claim 13, wherein the second conductive pattern comprises upper lead portions at least one of which is to be connected to the semiconductor chip as the upper conductor.